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SPECIFICATION

DEVICE SPECIFICATION for
TFT LCD Module
(1080× RGB × 1920 dots)

Model No.

LS050T1SX12 (K)

SCIC 2015-02-06 发行

CUSTOMER'S APPROVAL

DATE

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○ The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

○ In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

○ Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

○ SHARP assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in these specification sheets.

○ Contact and consult with a SHARP sales representative for any questions about this device.

[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.
There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth:$1\times10^{8}\Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

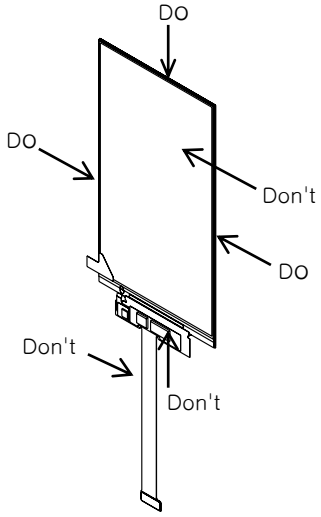
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

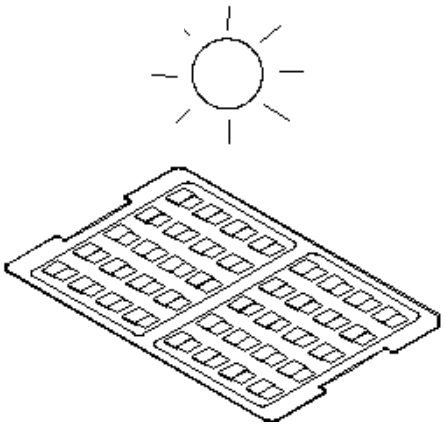
(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C, 60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
(3) Keeping Method

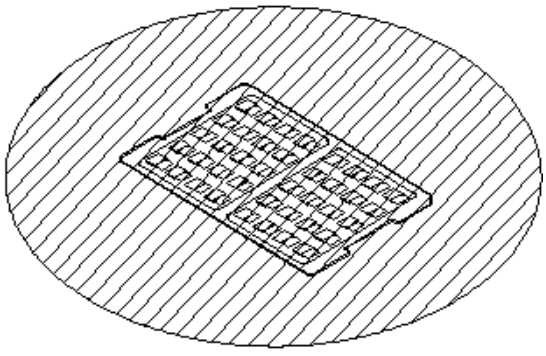
a. Don't keeping under the direct sunlight.

DON'T



b. Keeping in the tray under the dark place.

DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDD-1V8/VSP/VSN-GND) are low when LCD module is working, place the de-coupling capacitor nearby LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) The connector used in this LCD module is the one Sharp have not ever used.
Therefore, please note that the quality of this connector concerned is out of Sharp's guarantee.

(9) Be sure to use a power supply with the safety protection circuit such as the fuse for excess voltage, excess current, electric discharge waveform and Latch-up occurring.

(10) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.

Be sure to confirm the component of them.

(11) This module is designed for OCA TP bonding. If you are changing TP system, please contact us.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of LS050T1SX12(K) active matrix 16,777,216color LCD module.
Main color LCD module is controlled by Driver IC(NT35595).
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components,
14 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

Outline: See page 29
Connection: Board to board connector (Molex, Plug: 504248-3410)
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimensions (typ)		64.041 (W) × 116.224 (H) × 1.063 (D) *2	mm
Main LCD Panel	Active area	61.641 (W) × 109.584(H)	mm
	Display format	1080(W) × RGB × 1920(H)	-
	Dot pitch	0.019/0.01905 (W) × 0.05705/0.0571 (H)	mm
	Base color *1	Normally Black	-
	Illumination mode	Transmissive	
Mass		About:13	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.
*2 The above-mentioned table indicates module sizes without some projections and FPC.

4. Electrical Absolute Maximum Ratings

Table 2 Ta=25 ℃

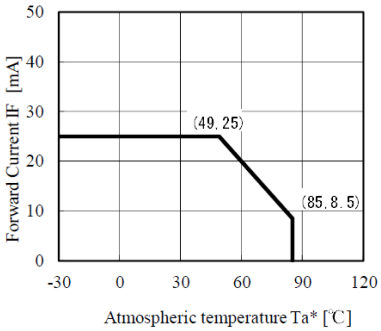
Parameter	Symbol	Conditions	Rated value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	VSP(AVDD)	Ta=+25℃	-0.3 ~ +6.5	V	【Note4-1,3】
Driver IC (Negative Analog) Power Supply Voltage	VSN(AVEE)	Ta=+25℃	+0.3 ~ -6.5	V	【Note4-1,3】
Driver IC (Digital) Power Supply Voltage	VDD-1V8(VDDIO)	Ta=+25℃	-0.3 ~ +5.5	V	【Note4-1,2】
LED Input electric current	ILED	—	20	mA	【Note4-4】

【Note4-1】If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.

【Note4-2】Make sure (High) VDD-1V8 ≥ GND (Low).

【Note4-3】Make sure (High) VSP ≥ AGND (Low), (Low) VSN≤AGND (High).

【Note4-4】Ambient temperature and the maximum input are fulfilling the following operating conditions.



Forward Current Derating Curve

5. Environment Conditions

Table 3

Item	Top		Tstg		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-20 ℃	+60℃	-30 ℃	+70℃	【Note5-1】
Humidity	【Note5-1】		【Note5-1】		No condensation

【Note5-1】Humidity:95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39°C (at Ta>40°C). Condensation of dew must be avoided.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

6. Electrical Specifications

(6-1) Power Supply Voltage Range

Table 4

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Positive Analog) Power Supply Voltage	VSP (AVDD)	5.4	5.5	5.6	V	【Note6-1】
Driver IC(Negative Analog) Power Supply Voltage	VSN (AVEE)	-5.4	-5.5	-5.6	V	【Note6-1】
Driver IC(Digital) Power Supply Voltage	V1P8 (IOVDD)	1.7	1.8	1.9	V	【Note6-1】

(6-2) DC characteristics

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic High level input voltage(Except RESX)	VIH	0.7 V1P8	-	V1P8	V	【Note6-1,2】
Logic Low level input voltage(Except RESX)	VIL	VSS	-	0.3V1P8	V	【Note6-1,2】
Logic High level input voltage(RESX)	VIH	0.8 V1P8	-	V1P8	V	【Note6-1,2】
Logic Low level input voltage(RESX)	VIL	VSS	-	0.2V1P8	V	【Note6-1,2】
Logic High level input voltage(ENPWRP/N)	VIH	0.7AVDD	-	AVDD	V	【Note6-1,2】
Logic Low level input voltage(ENPWRP/N)	VIL	AVSS	-	0.3AVDD	V	【Note6-1,2】
Logic High level output voltage	VOH	0.8 V1P8		V1P8	V	【Note6-1,2,3】
Logic Low level output voltage	VOL	VSS		0.2 V1P8	V	【Note6-1,2,3】
Logic High level leakage MIPI	ILIH			10	μA	Vin = 0 to 1. 3 V
Logic Low level leakage MIPI	ILIL	-10			μA	Vin = 0 to 1. 3 V
Current consumption	IVSP	-	7.70	10.37	mA	【Note6-4】
	IVSN	-	8.23	12.16	mA	【Note6-4】
	IV1P8	-	25.05	32.83	mA	【Note6-4】
	IVSP	-	0.004	0.02	mA	【Note6-5】
	IVSN	-	0.004	0.02	mA	【Note6-5】
	IV1P8	-	0.004	0.02	mA	【Note6-5】

【Note6-1】VDDI=1.65 to 3.6V, VCI= 2.5 to 4.8V, VDDAM=1.65 to 3.6 V, AVDD=4.5 to 6.0V, AVEE=-6.0 to -4.5V, AVSS=VSS=0V,Ta=-30 to 75 (to +85 no damage)

【Note6-2】When the measurements are performed with LCD module, Measurement Points are like below. CSX, WRX, DCX, RESX, IM[2 : 0] and Test pins

【Note6-3】IOH = -0.1mA IOL = +0.1mA

【Note6-4】Measurement Conditions : Full screen white pattern, AVDD/AVEE=(+/-)5.50V,IOVDD=1.80V, 60Hz Refresh, MIPI-DSI Video Bypass Mode

【Note6-5】Measurement Conditions : Deep standby mode

(6-3) MIPI DSI characteristics

<DC characteristics>

Table6 Ta=+25°C, GND=0V

Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.65	1.8	3.6	V
VP_HSSI	High speed / Low power mode operating voltage		1.2		V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
|VOD|	HS transmit differential voltage (VOD=VDP-VDN)	140	200	250	mV
V_{IDTH}	Different input high threshold			70	mV
V_{IDTL}	Different input low threshold	-70			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
VGNDSH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0.0		550	mV
VIH	Logic 1 input threshold	880		VDDAM	mV
VHYST	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD,MAX	Logic 0 contention threshold	0.0		200	mV
VILCD,MIN	Logic 1 contention threshold	450		VDDAM	mV

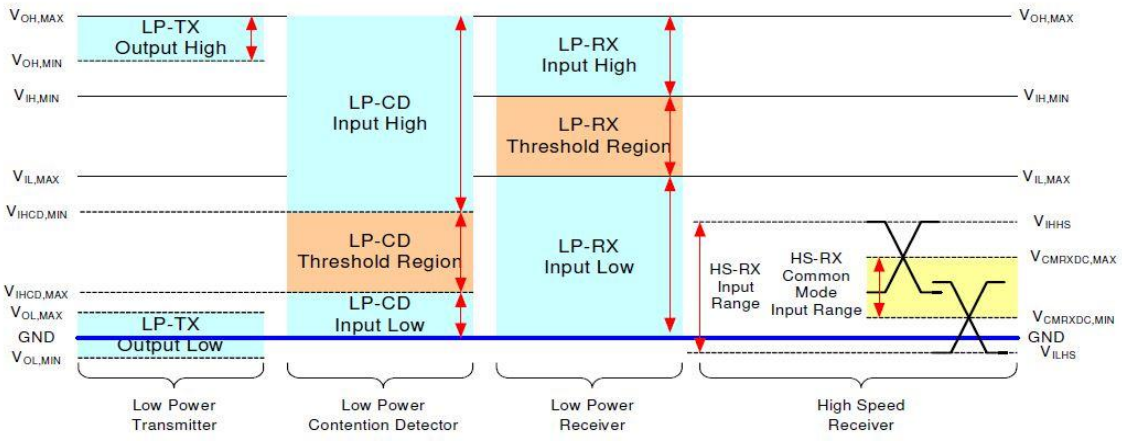


Fig.1

<AC Characteristics>
MIPI Interface Characteristics
High Speed Data Transmission: Data-Clock Timing

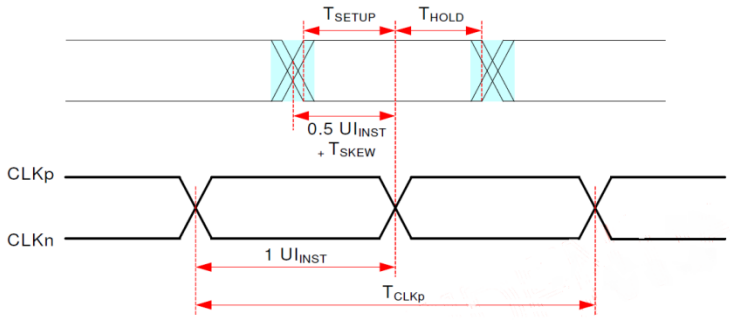


Fig.2

Table 7

Ta=+25°C, GND=0V

Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2,10
Data to Clock Skew [measured at tansmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	3
		-0.2		0.2	UI_{INST}	4
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
Data to Clock Hold Time [measured at reciever]	T_{HOLD}[RX]	-0.15		0.15	UI_{INST}	5
		-0.2		0.2	UI_{INST}	6
20% -80% rise time and fall time	t_R / t_F	100			ps	9
				0.3	UI_{INST}	7
				0.35	UI_{INST}	8

Note:

1. This value corresponds to a minimum 80 MHz data rate.
2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.
3. Total silicon and package delay budget of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.
4. Total silicon and package delay budget of 0.4* UIINST when D-PHY is supporting maximum data rate > 1Gbps.
5. Total setup and hole window for receiver of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.
6. Total setup and hole window for receiver of 0.4* UIINST when D-PHY is supporting maximum data rate > 1Gbps.
7. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).
8. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).
9. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.
10. For MIPI speed limitation:

[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 3Gbps for 6-6-6; and 2.67Gbps for5-6-5.

< HS Data Transmission >

High-Speed Data Transmission in Bursts

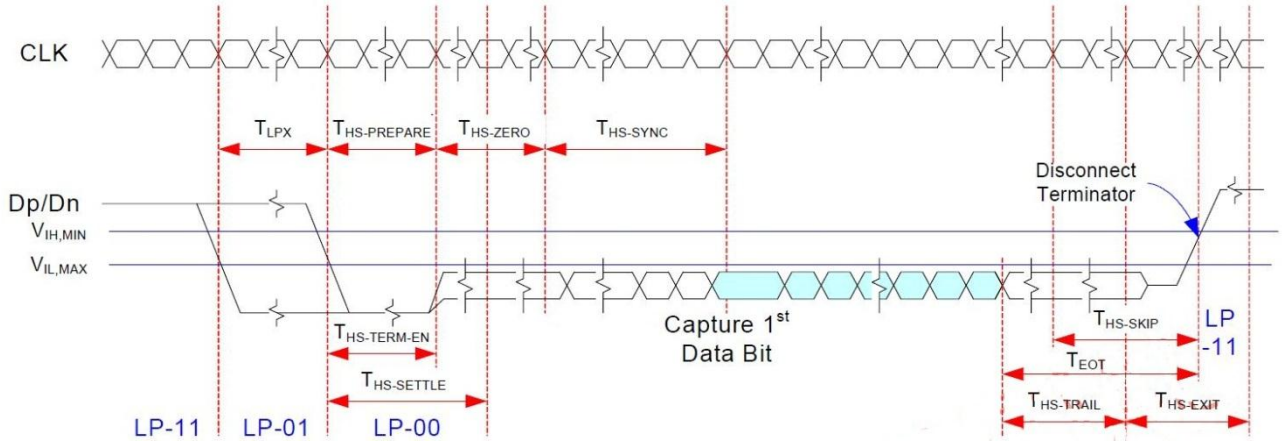


Fig.3

Table 8

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of Ths-TRAIL or Tclk-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{Hs-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	THS-SKIP	40		55+4UI	ns
Time to drive LP-11 after HS burst	THS-EXIT	100			ns
Length of any Low-Power state period	TLPX	50			ns
Sync sequence period	THS-SYNC		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	THS-ZERO	105+6UI			ns

Note:

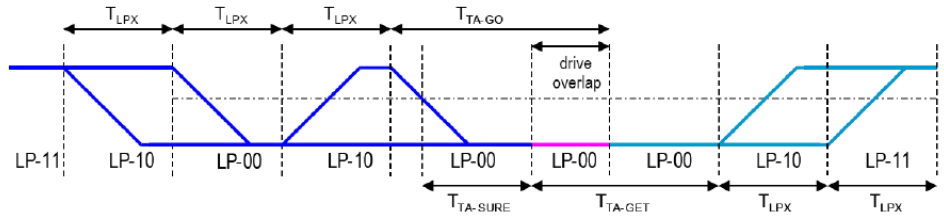
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.

3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

< Turnaround Procedure>

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Fig.4

<Switching the Clock Lane between Clock Transmission and Low-Power Mode>

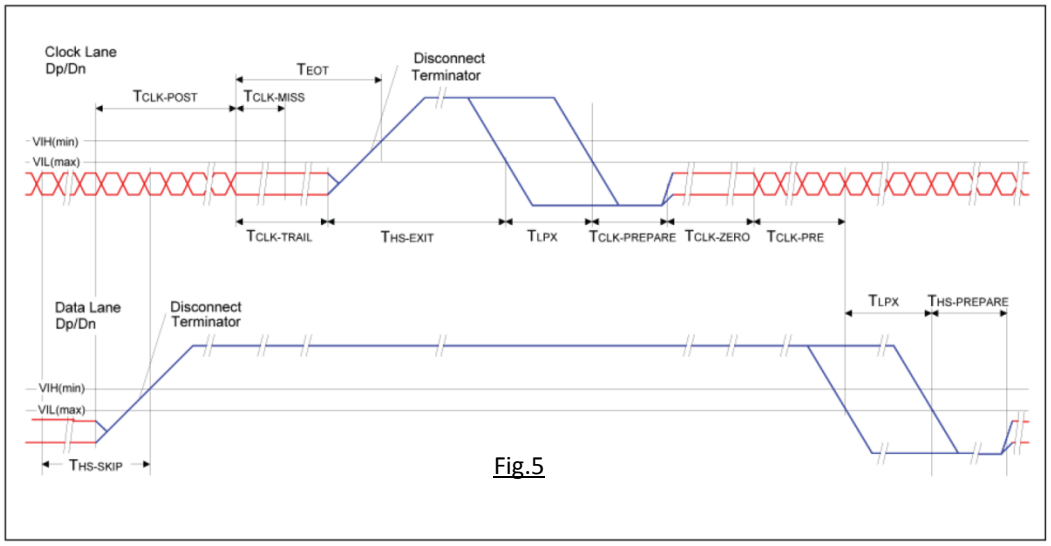


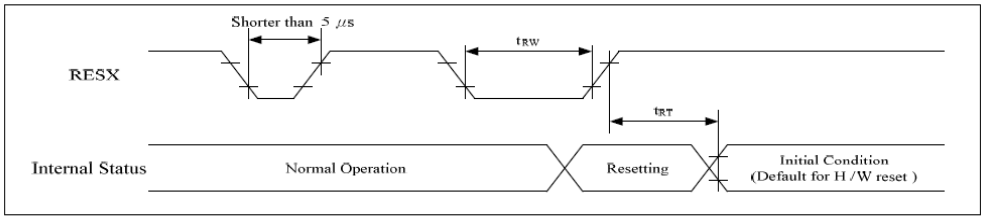
Fig.5

Table 8-1

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+112UI			ns
Detection time that the clock has stopped toggling	TCLK-MISS			60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38		95	ns
Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE +TCLK-ZERO	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	TCLK-PRE	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60			ns

Note:
1. Due to this value need to correspond with a minimum 80 MHz data rate, so the minimum TCLK-POST is "60ns+112UI".

(6-4) Reset Timing Characteristics



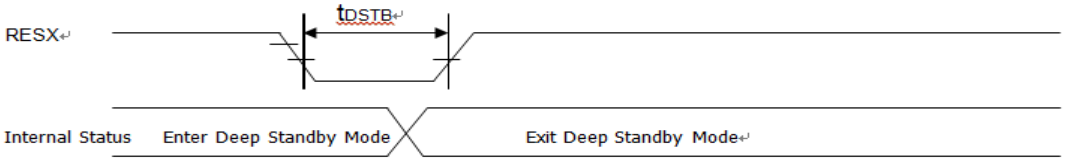


Fig.6

Table 8-2

Reset Timing Characteristics VCI=2.5~4.8V, IOVCC=1.65~3.6V, VDDAM=1.65~3.6V					
Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10(Note)	-	us
	tRT	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms
	tDSTB	Reset pulse duration	3	-	ms

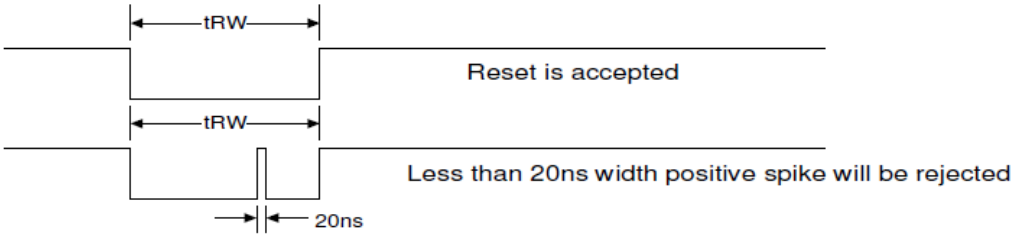
Note:
-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers.
This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.

-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below:



-When Reset applied during Sleep-In Mode.
-When Reset applied during Sleep-Out Mode.

-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

(6-5). Vertical Timing Characteristics

Table 9 Ta=+25°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Refresh frame rate operation range	Rfror	57	60	63	Hz	
Refresh frame rate tolerance	Rfrt	-5	-	-	%	

*Command mode in still image 60Hz self-refresh

(6-6) LED backlight

At main panel the back light uses 14pcs edge light type white LED.

Table 10

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward current	Ta=25 °C	I_{LED}	-	20	25	mA	LEDA-LEDK
Number of LED components	14 pcs LED (7 pcs serial X 2 parallel)						

*Please consider Allowable Forward Current on used temperature

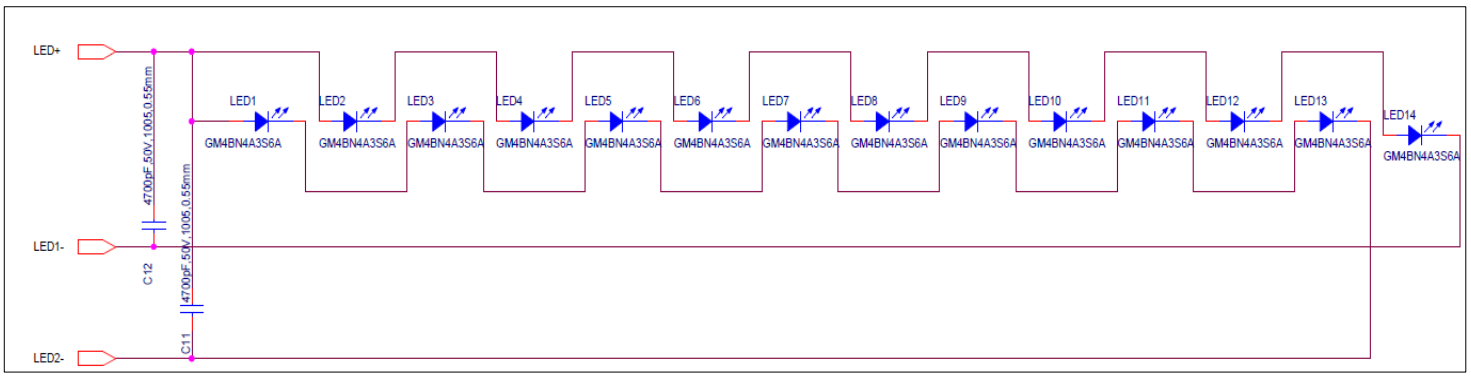


Fig.7 Schematics drawing of backlight

(6-7) Interface signals

Table 11

Pin No.	Symbol	I/O	Description	Remarks
1	HSOUT	O	Signal to synchronize LCD driver and touch panel controller. (Horizontal scan)	
2	LED-CATHODE1	-	LED back light power group1 negative	
3	GND	-	Ground	
4	LED-CATHODE2	-	LED back light power group2 negative	
5	LANE3-N	I	MIPI data3 negative signal	
6	NC	-	Not connect	
7	LANE3-P	I	MIPI data3 positive signal	
8	LED-ANODE	-	LED back light power positive	
9	GND	-	Ground	
10	GND	-	Ground	
11	LANE0-N	I/O	MIPI data0 negative signal	
12	V1P8	I	Power supply for I/O(1.8V)	
13	LANE0-P	I/O	MIPI data0 positive signal	
14	VSP(AVDD)	I	Power supply for analog(+5.5V)	
15	GND	-	Ground	
16	VSP(AVDD)	I	Power supply for analog(+5.5V)	
17	CLK-N	I	MIPI clock negative signal	
18	VSN	I	Power supply for analog(-5.5V)	
19	CLK-P	I	MIPI clock positive signal	
20	VSN	I	Power supply for analog(-5.5V)	
21	GND	-	Ground	
22	GND	-	Ground	
23	LANE1-N	I	MIPI data1 negative signal	
24	LCD-ID-DET1	-	ID1(GND)	
25	LANE1-P	I	MIPI data1 positive signal	
26	LCD-ID-DET0	-	ID0(GND)	
27	GND	-	Ground	
28	RESET	I	Device reset signal	
29	LANE2-N	I	MIPI data2 negative signal	
30	LCD-TE	O	Tearing signal output from driver IC	
31	LANE2-P	I	MIPI data2 positive signal	
32	CABC	-	Backlight LED driver PWM	
33	GND	-	Ground	
34	GND	-	Ground	

Notes:The direction is named with respect to the display module, I = from host to LCM, O = from LCM to host.

Table 12 Connector description

Assembled on	Item	Description
Phone PWB	Connector type	Board to Board
	Pin amount	34
	Manufacturer	MOLEX
	Details	Rec:504208-3410

(6-8) General Timing Diagram

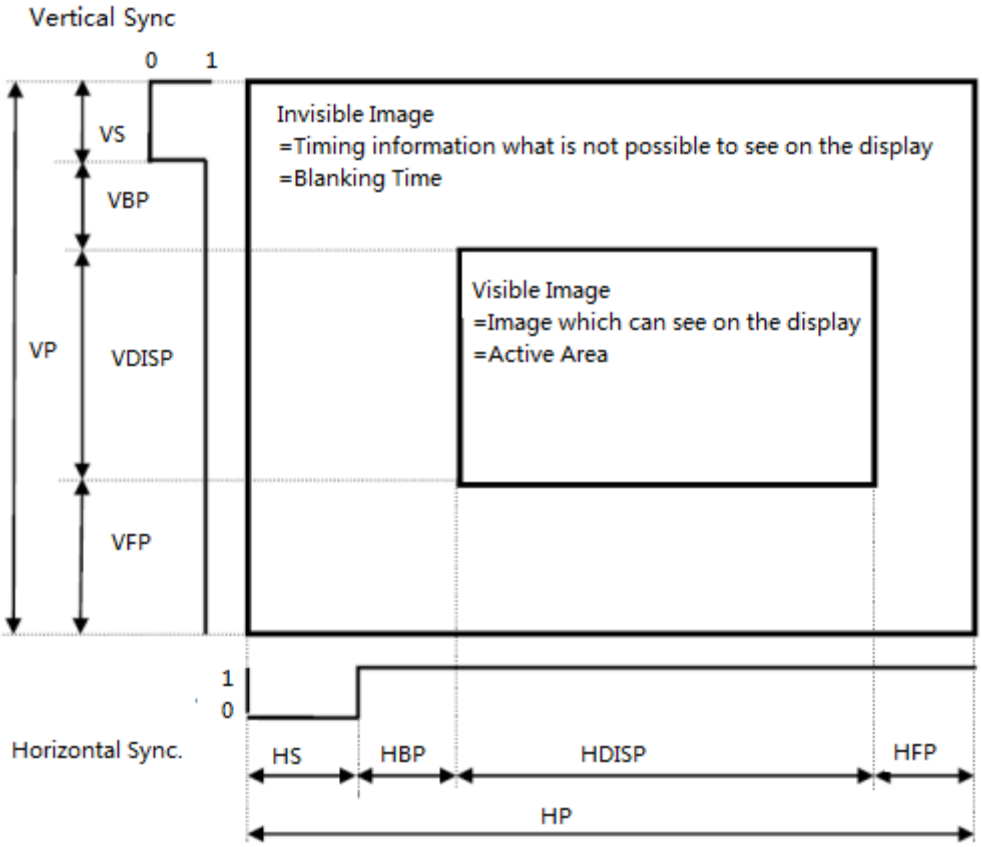


Fig.8

(6-9) Vertical Timing

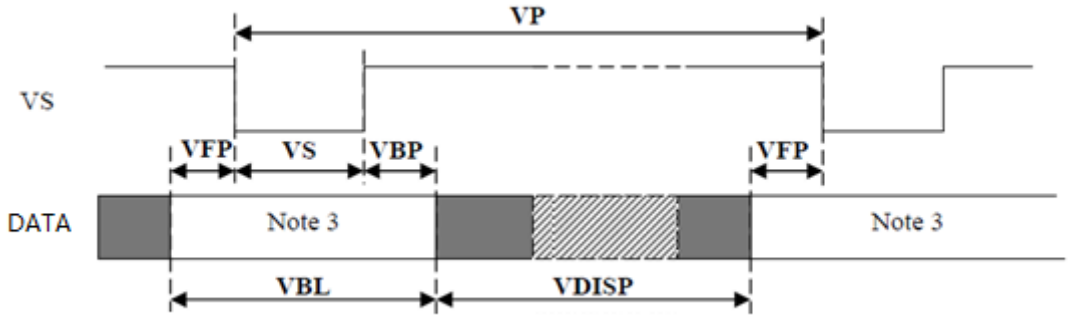


Fig.9

Table 13

Item	Symbol	Conditions	Min	Recommend	Max	Unit
Vertical cycle	VP		-	1930	-	Line
Vertical low pulse width	VS		2	2	-	Line
Vertical front porch	VFP		4	4	-	Line
Vertical back porch	VBP		2	4	-	Line
Vertical data start point		VS+VBP	4	6	-	Line
Vertical blanking period	VBL	VFP+VS+VBP	8	10	-	Line
Vertical active area		VDISP	-	1920	-	Line
Vertical Refresh Rate	VRR		-	60	-	Hz

Ta = -20 °C ~ +60°C, V1P8= 1.8 V, VSP=5.5V, VSN=-5.5V, GND = 0 V

(6-10) Horizontal Timing

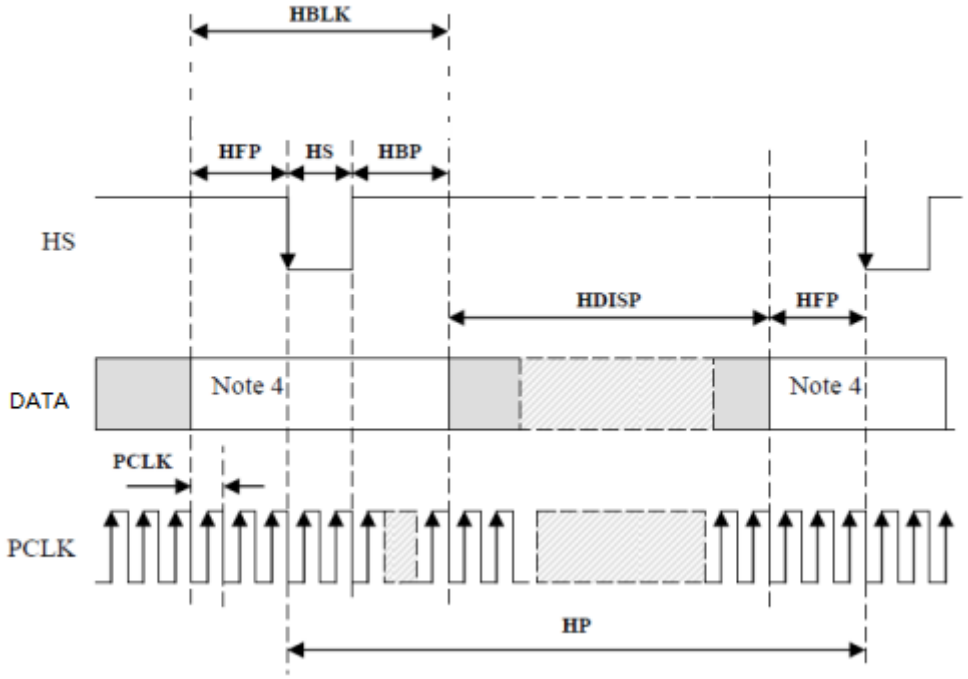


Fig.10

Table 14

Item	Symbol	Conditions	Min	Recommend	Max	Unit
HS cycle	HP		-	1242	-	PCLK
HS low Pulse width	HS		-	10	-	PCLK
Horizontal back porch	HBP		16	50	-	PCLK
Horizontal front porch	HFP		12	102	-	PCLK
Horizontal data start point		HS+HBP	16	60	-	PCLK
Horizontal blanking period	HBLK	HFP+HS+HBP	28	162	-	PCLK
Horizontal active area	HDISP		-	1080	-	PCLK
1 Horizontal timing			8.649	8.649	-	us
Pixel clock frequency	PCLK		-	6.96	-	ns
			-	143.6	-	MHz
MIPI Speed(4 lane)	-	-	880	-	1000	Mbps/lane

Ta = -20°C ~+60°C, V1P8= 1.8 V, VSP=5.5V, VSN=-5.5V, GND = 0 V

(6-11) Schematic of LCD module system

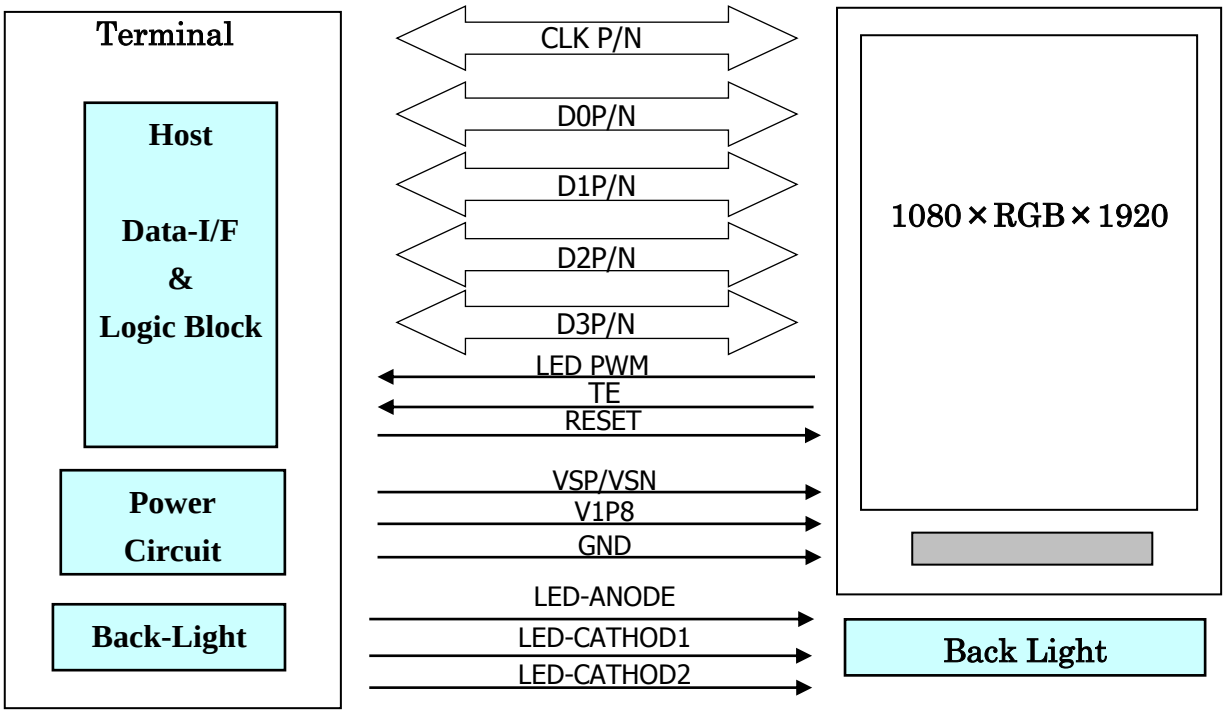


Fig.11 Schematic of LCD module system

7. Initial Sequence

(7-1) Power ON sequence

Fig.12

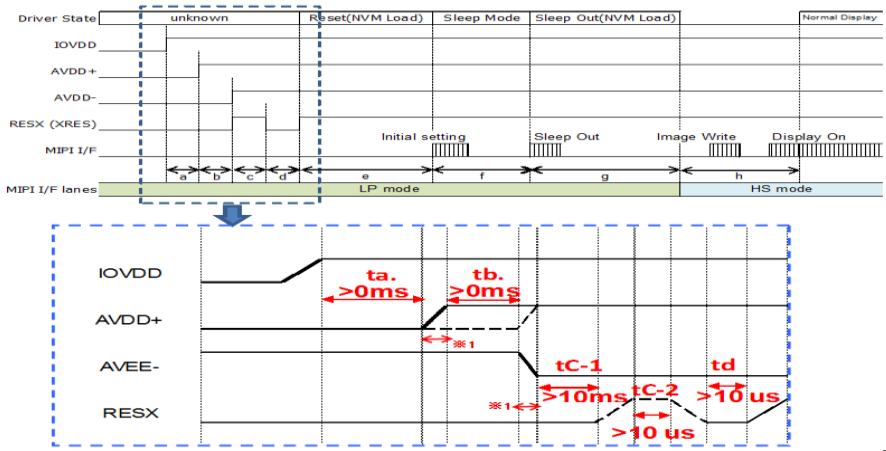


Table 15

Recommended Power On Sequence for NT35595								term
Step	Address	Parameter	Data	DSI data type		Delay	Command	
1	Initial condition						XRES = L	
2	Power Supply IOVCC (Typ1.8V)						IOVDD ON	
3	Wait					Min.>0 ms	(a.)Wait until IOVDD power stable	a.
4	Power Supply VSP (Typ5.5V)						AVDD+ ON	
5	Wait					–	(b.)Wait until AVDD+ power stable	b.
6	Power Supply VSN (Typ-5.5V)						AVDD- ON	
7	Wait					Min.10 ms	(c.)Wait until AVDD- power stable	c-1.
8	RESX High						XRES = H	
9						Min.10us		c-2.
10	RESX go Low						XRES = L	
11						Min.10us		d.
12	RESX go Hi						XRES = H	
13	Wait					Min.10 ms	[Automatic] NVM Auto load	e.
14							[Automatic] Sleep Mode On	
15	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
16	[CMD1]0xBB	P1	**h	DCS	15h		Set MIPI Display Mode 0x03(VIDEO Mode, GRAM acceces disable) 0x10(Command Mode, GRAM acceces enable) 0x13(VIDEO Mode, GRAM acceces enable)	f.
17	[CMD1]0xB0	P1	03h	DCS	15h		CRC/ECC function 00h : ON , 03h : OFF	
18 (note1)	[CMD1]0x3B	P1 P2 P3 P4 P5	03h 06h 04h 3Ch 66h	DCS	39h		Setup RGB-MIPI-Video-Mode Signal Control Notice:If using the MIPI VIDEO Mode(0xBB=0x03), DSI Video Mode Packet Stream timing is necessary. 1. VFP / VBP timing must be set the same as CMD1 Reg 0x3B. 2. HBP / HFP timinng must be set the same as CMD1 Reg 0x3B. 3. 1 H line Timing must be longer(or equal) than 1H=**8.643**us.	
19	If customer need, please add initial command in here.							
20	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
21	[CMD1]0x35	P1	00h	DCS	15h		TE ON	
22	[CMD1]0x11	-	-	DCS	05h		Sleep Out	g.
23	Wait					Min.100ms		
24							[Automatic] Sleep Mode Off	
25	[CMD1]0x51	P1	FFh	DCS	15h		SET LED PWM full duty	h.
26 (note2)	[CMD1]0x53	P1	**h	DCS	15h		SET LED PWM control 24h → Backlight control ON 20h → Backlight control OFF	
27 (note2)	[CMD1]0x55	P1	**h	DCS	15h		SET CABC control 81h: CABC on(UI mode) 82h: CABC on(Still mode) 83h: CABC on(Moving mode)	
28	[CMD3]0xFF	P1	F0h	DCS	15h		NVT Command	
29	[CMD3]0x92	P1	01h	DCS	15h		Software solutuin for ESD issue	
30	[CMD3]0x13	P1	01h	DCS	15h		Software solution for CUT4(abnormal dot)	
31	Display data transfer						Image Write	
32	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
33	[CMD1]0x29	-	-	DCS	05h		Display On	
34	Wait					Min.40 ms		
35							[Automatic] Display On	
36	Backlight on							

NOTE1: STEP18 can be deleted if command mode is used.
NOTE2: Please make sure set SRE,CE,CABC all off(not set step25-27) when module is under optical inspection(TP attach,set assembly).
CE sequnce contains no MTP parameters, will be provide otherwise.
NOTE3: The above sequence applies on the premise of MIPI Command mode,if MIPI Video mode has been used,
please set the step31 after step22.
※1 With the destination of avoiding latch-up issue, two sequence is proposed for select:
1. AVDD+/AVDD- slope time should set >1ms.
2. AVDD+ on → AVDD- on(fig **tb** time) should set > 1ms and AVDD+ /AVDD- Slope time > 0.2ms

(7-2) Power OFF sequence

Fig.13

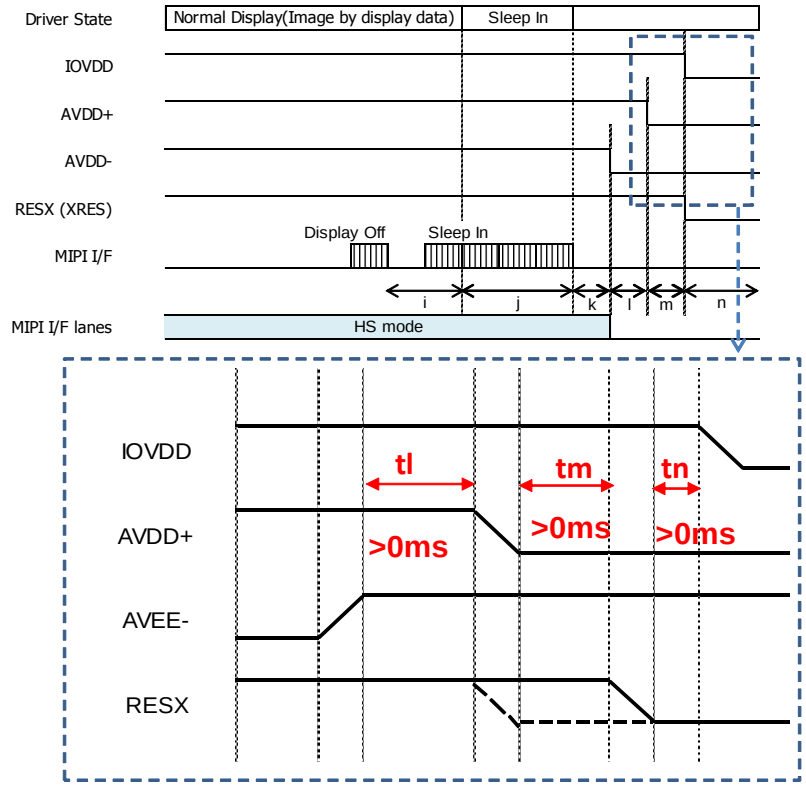


Table 16

Recommended Power Off Sequence for NT35595								term
Step	Address	Parameter	Data	DSI data type		**Delay**	**Command**	
1	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
2	28h	-	-	DCS	39h		Display Off	i
3	Wait					Min.1 frame		
4	10h	-	-	DCS	39h		Sleep In	j
5	Wait					Min. 4frame	Hsync/Vsync signals should be send after Sleep In command	
6							Mipi data transfer Stop	k
7	Wait					Min.0ms		
8	VSN(Typ-5.5V) OFF							l
9						Min.>0ms	Wait until AVDD- power stable	
10	VSP(Typ+5.5V) OFF							m
11						Min.>0ms	Wait until AVDD+ power stable	
12	RESX Low						XRES = L	n
13						Min.>0ms	Wait until RESX power stable	
14	IOVCC OFF(Typ1.8V) OFF							

(7-3)Deep standby In Sequence

Table 17

Recommended Deepstandby in Sequence for NT35595								
Step	Address	Parameter	Data	DSI data type		Delay	Command	term
1	28h	-	-	DCS	39h		Display Off	
2	Wait					Min.1 frame		
3	10h	-	-	DCS	39h		standby In	
4	Wait					Min. 4frame	Hsync/Vsync signals should be send after Sleep In command	
5							Mipi data transfer Stop	
6	4Fh	p1	01h	DCS		Min.0ms	Enter Deepstandby Mode	
7	Keep RESX =Hi, Pull MIPI signals with VSS, Keep IOVCC/VSP/VSN Power							

(7-4)Deep standby Out Sequence (Deep standby In -> Normal)

Table 18

Recommended Deepstandby Out Sequence for NT35595								
Step	Address	Parameter	Data	DSI data type		Delay	Command	term
1	RESX go Low						XRES = L	
2	Wait					Min.3ms		
3	RESX go Hi						XRES = H	
4	Wait					Min.10 ms	[Automatic] NVM Auto load	
5	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
6	[CMD1]0xBB	P1	**h	DCS	15h		Set MIPI Display Mode 0x03(VIDEO Mode, GRAM acceces disable) 0x10(Command Mode, GRAM acceces enable) 0x13(VIDEO Mode, GRAM acceces enable)	
7	[CMD1]0xB0	P1	03h	DCS	15h		CRC/ECC function 00h : ON , 03h : OFF	
8 (note1)	[CMD1]0x3B	P1 P2 P3 P4 P5	03h 06h 04h 3Ch 66h	DCS	39h		Setup RGB-MIPI-Video-Mode Signal Control Notice:If using the MIPI VIDEO Mode(0xBB=0x03), DSI Video Mode Packet Stream timing is necessary. 1. VFP / VBP timing must be set the same as CMD1 Reg 0x3B. 2. HBP / HFP timinng must be set the same as CMD1 Reg 0x3B. 3. 1 H line Timing must be longer(or equal) than 1H=**8.643**us.	
9	If customer need, please add initial command in here.							
10	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
11	[CMD1]0x35	P1	00h	DCS	15h		TE ON	
12	[CMD1]0x11	-	-	DCS	05h		Sleep Out	
13	Wait					Min.100ms		
14							Exit Deepstandby	
15	[CMD1]0x51	P1	FFh	DCS	15h		SET LED PWM full duty	
16 (note2)	[CMD1]0x53	P1	**h	DCS	15h		SET LED PWM control 0x24 → Backlight control ON 0x20 → Backlight control OFF	
17 (note2)	[CMD1]0x55	P1	**h	DCS	15h		SET CABC control 81h: CABC on(UI mode) 82h: CABC on(Still mode) 83h: CABC on(Moving mode)	
18	[CMD3]0xFF	P1	F0h	DCS	15h		NVT Command	
19	[CMD3]0x92	P1	01h	DCS	15h		Software solutuin for ESD issue	
20	[CMD3]0x13	P1	01h	DCS	15h		Software solution for CUT4(abnormal dot)	
21	Display data transfer						Image Write	
22	[CMD1]0xFF	P1	10h	DCS	15h		Command Page select CMD1	
23	[CMD1]0x29	-	-	DCS	05h		Display On	
24	Wait					Min.40 ms		
25							[Automatic] Display On	
26	Backlight on							

NOTE1: STEP8 can be deleted if command mode is used.
NOTE2:Please make sure set SRE,CE,CABC all off(not set step15-17) when module is under optical inspection(TP attach,set assembly).
CE sequnce contains no MTP parameters, will be provide otherwise.
NOTE3: The above sequence applies on the premise of MIPI Command mode,if MIPI Video mode has been used,
please set the step21 after step12.

8. Optical Characteristics

Table 19 VDD-1V8=1.8 V, VSP=5V, VSP=-5V, ILED=20mA, Ta = 25℃

Optical Characteristics							
Parameter	symbol	condition	MIN	TYP	MAX	unit	Remark
Brightness	Br	θ=0°	345	460	-	cd/㎡	Note1,2
Contrast	Co	θ=0°	700	1000	-		Note1,3
Viewing Angle	θ11	CR > 10	85	-	-	deg	Note1
	θ12		85	-	-		
	θ21		85	-	-		
	θ22		85	-	-		
Response Time	(τr+td)	θ=0°	-	-	35	ms	Note1,4
White chromaticity	x	θ=0°	0.27	0.3	0.33		Note.1,3
	y		0.29	0.32	0.35		
Red	x	θ=0°	0.647	0.682	0.717		Note.1,3
	y		0.275	0.310	0.345		
Green	x	θ=0°	0.243	0.278	0.313		Note.1,3
	y		0.631	0.666	0.701		
Blue	x	θ=0°	0.117	0.152	0.187		Note.1,3
	y		0.003	0.038	0.073		
Uniformity	-	θ=0°	80%	85%	-	%	Note.5
NTSC ratio	-	θ=0°	-	95%	-	%	Note.1
Flicker	F	θ=0°	-	-	10	%	Note.6
Crosstalk	CT	θ=0°	-	-	4.5	%	Note.7

Note 1) Definition of range of visual angle

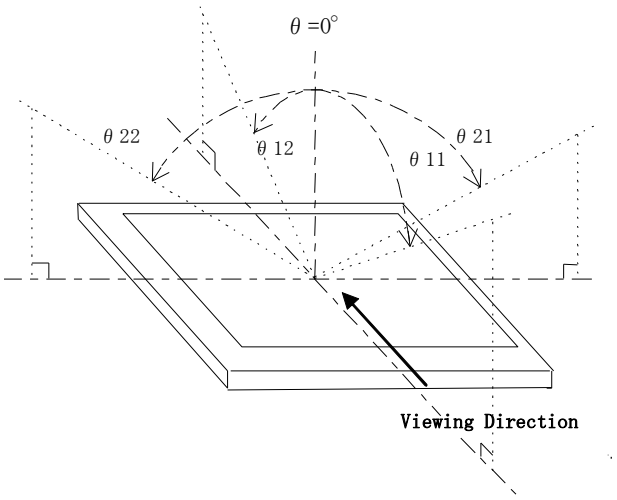


Fig.14 Definition of viewing angle

Note 2) Brightness is measured as shown in Fig.14, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

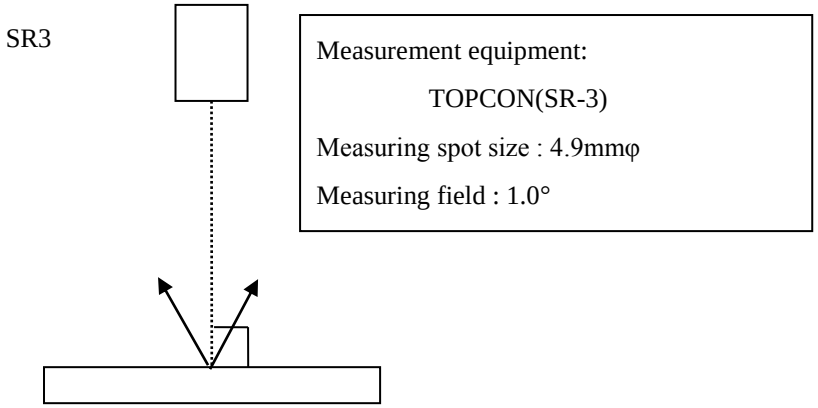


Fig.15 Optical characteristics Test Method (Brightness)

Note 3) Contrast ratio is defined as follows:

$$Co = \frac{Luminance(brightness) allpixcels "White"}{Luminance(brightness) allpixcels "Black"}$$

Note 4) Response time is defined as follows:

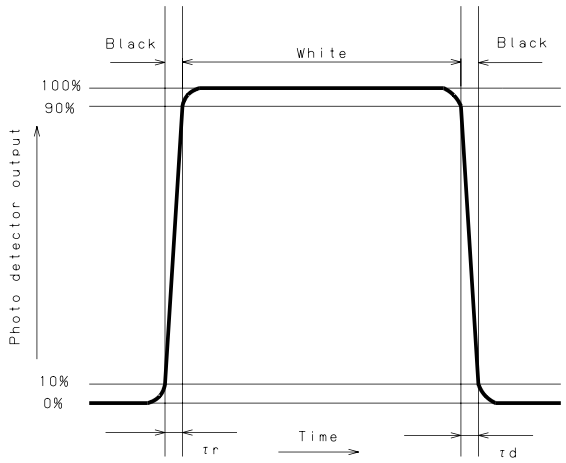


Fig.16 Response time

Note 5) Uniformity is defined as follows:

$$Uniformity = \frac{Minimum\ Luminance(brightness)\ in\ 9\ points}{Maximum\ Luminance(brightness)\ in\ 9\ points}$$

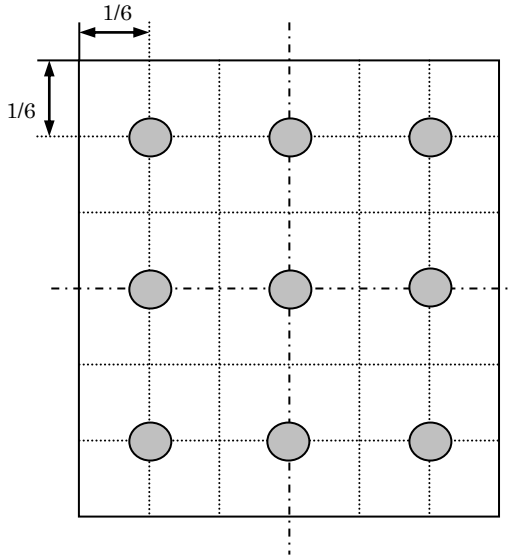


Fig.17 Measuring Point

Note 6) Flicker is defined as follows:

- ·Measuring systems: YOKOGAWA 3298_01 + 3298_11
- ·Temperature = 25℃(±3℃), Frame Frequency = 60Hz, LED back-light: ON, Environment brightness < 150 lx
- ·Measurement point is panel center.
- ·Conversion of Flicker ratio : Flicker[%] =ACrms/DC×100
- ·Measured sample : New sample before a long term aging.
- ·Flicker ratio is very sensitive to measuring condition.

Note 7) Crosstalk is defined as follows:

$CT=|Yw(Xi)-YG(Xi)|\times 100(\%)/YG(Xi)$ X=U,D,L,R i=gray 127

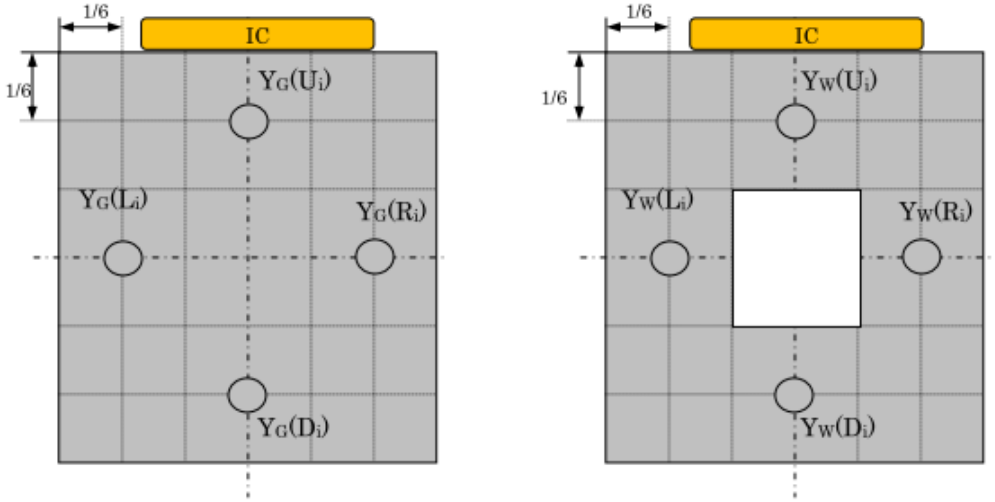


Fig.18 Measuring Point

9. Reliability

Table.20

No.	Test	Condition	Judgment criteria
1	Temperature Cycling	-30℃ → 70℃ … 30min(3min)30min 50cycle	Per table in below
2	Humidity Storage	Ta=60℃ 90%RH 240h	Per table in below
3	High Temp. Storage	Ta= 70℃ 240h	Per table in below
4	Low Temp. Storage	Ta=-30℃ 240h	Per table in below
5	Humidity Operation	Ta=40℃ 90%RH 240h	Per table in below (polarizer discoloration is excluded)
6	High Temp. Operation	Ta= 60℃ 240h	Per table in below
7	Low Temp. Operation	Ta=-20℃ 240h	Per table in below
8	ESD	Discharge resistance: 0 Ω Discharge capacitor: 200 pF Discharge voltage: ±200 V Max Discharge 1 time to each input line ※ "GND" of display module is connected GND of test system ground.	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

10. Packaging specifications

(10-1) Details of packaging

1) Packaging materials: Table.22
2) Packaging style : Fig.19, 20

(10-2) Reliability

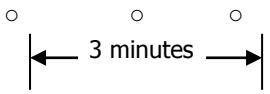
1) Vibration test

Table.21

Item	Test			
Frequency	5 Hz to 50 Hz (3 minutes cycle)			
Direction	Up-Down, Left-Right, Front-Back (3 directions)			
Period	Up-Down	Left-Right	Front-Back	Total
	60min	15min	15min	90min

The frequency should start at 5 Hz and vary continuously.

Total amplitude	20mm	0.2mm	20mm	0.2mm	
Frequency	5 Hz	50 Hz	5 Hz	50 Hz	(For 9.8m/s^2)



2) Drop test

Drop height: 750mm
Number of drop: 10 times (Drop sequence: 1 corner, 3 edges, 6 faces)

(10-3) Packaging quantities

120 modules per master carton

(10-4) Packaging weight

About: 5.7kg

(10-5) Packaging outline dimensions

365mm×580mm×187mm

(Packaging materials)

Table.22

	Parts name	CRITERION(after test)
1	Master carton	Corrugate card board
2	Inside sleeve	Corrugate card board
3	Outside sleeve	Corrugate card board
4	Tray for packaging	Polystyrene with anti-static treatment +anti-static polystyrene
5	Protective bag	Polystyrene with anti-static treatment
6	OPP tape	Polypropylene
7	Bar code label	anti-static polystyrene

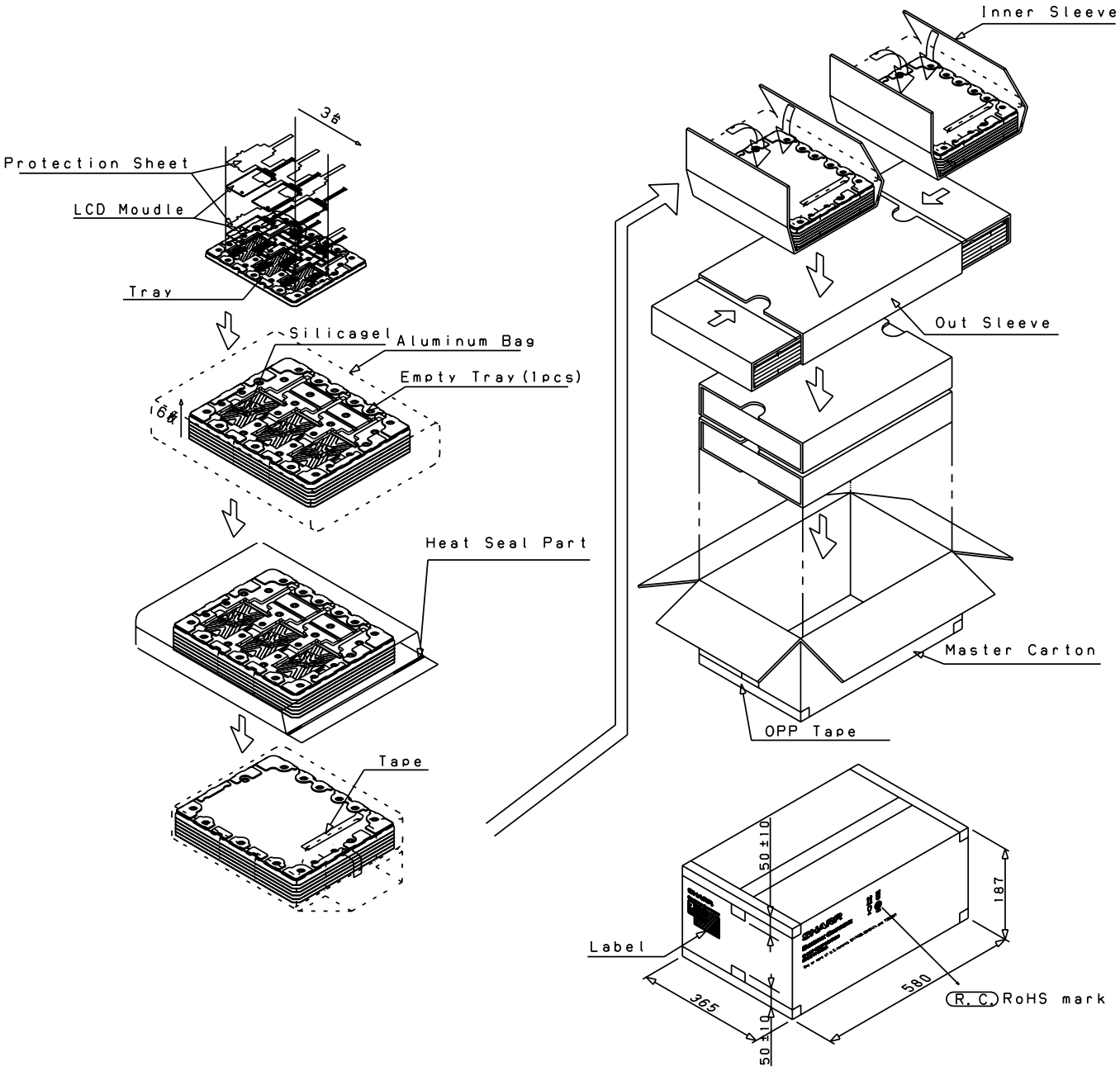


Fig.19 Packaging style (Tray for packaging)

Bar code label

Fig.20 **Packaging style (Master carton for packaging)**

11. Serial Number Label identification

Numbering is specified as follows.

3 X 0000001 A Q

①② ③ ④⑤

① product year (lower 1 digits)

3: 2013

4: 2014

② product month

1: January
2: February
3: March
:
9: September
X: October
Y: November
Z: December

③ serial number

0000001 ～ 9999999

④ Version number

⑤ factory code

12. Outline dimensions

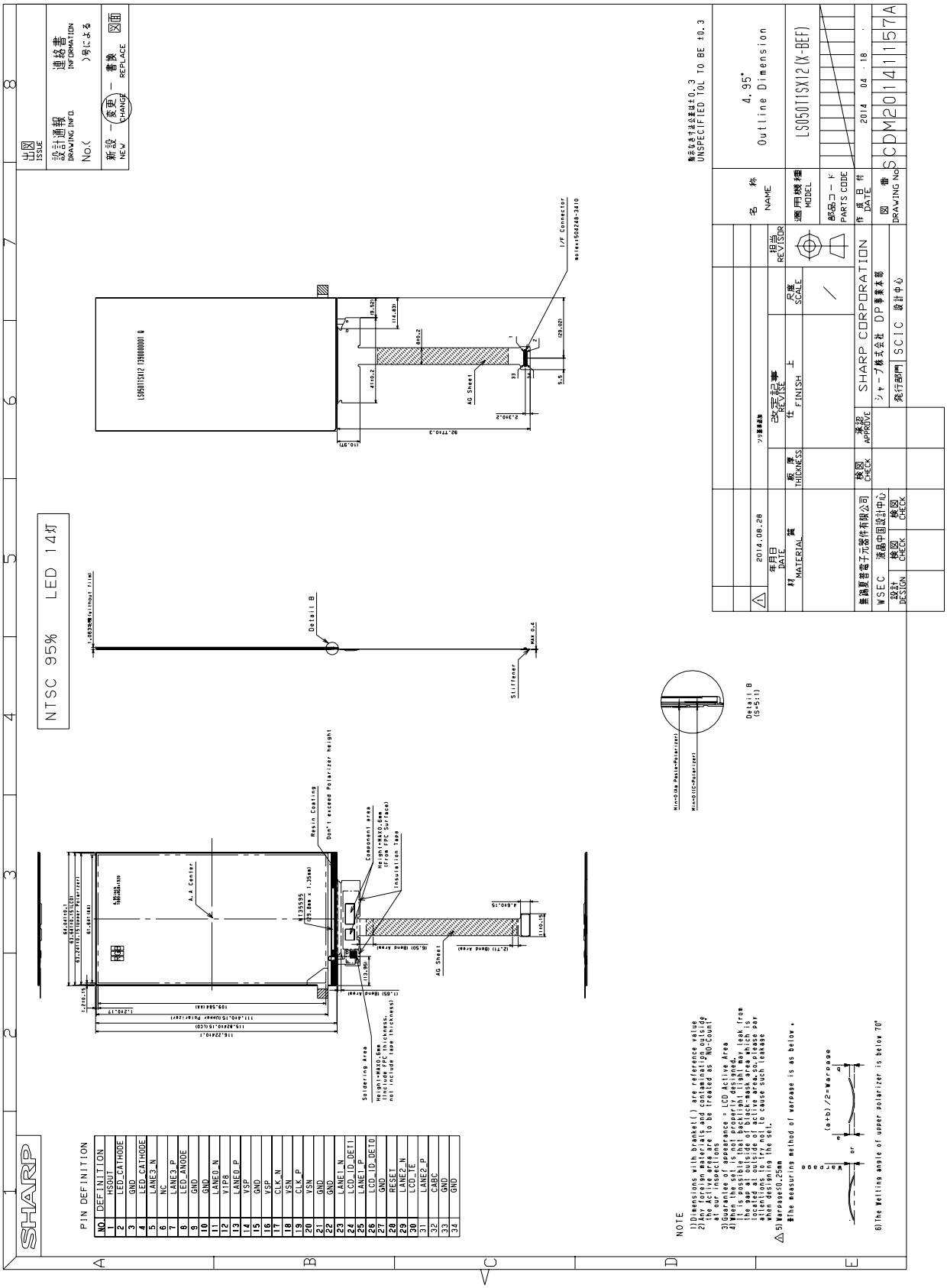


Fig. 21 Outline dimensions